The CD-951V3 is a 360°-voltage controlled phase shifter in the frequency range of 100 Hz to 200 kHz, and adopts CMOS-level (0/+5 V) square wave for input and output. This is composed of the ±100°-variable voltage controlled phase controlled circuit and 50% duty circuit with 0/180° switch. The combination use of the ±100°-phase shifter and 0/180°-selector enables the output of 50% duty square wave that phase is shifted in the 360° range to the phase shifter input signal.

Double frequency is produced by the 50% duty input signal if 2f mode is placed through the connection with the specified pin. The CD-951V3 is in a 6-surface shielded 20-pin single inline package (SIP), which is a great contributor to the implementation of high precision signal processing and high density mounting.

### Absolute maximum ratings
- **Supply voltage** (±Vs): ±1.8 V
- **Phase control DC input voltage** (V(IN)): ±Vs
- **Phase shifter input voltage** (SHIFTER IN): −0.5 V to +5.5 V
- **Logic control input voltage**: −0.5 V to +5.5 V

### 50%-duty output/voltage controlled phase shifter

#### I/O Setting
- **I/O pin**: Input: Pin 14, Output: Pin 18
- **Setting**: Pins 15-16 shorted, Pin 17 open
- **I/O characteristics**: The square wave of duty ratio 50% which did phase shifting by Vc IN is output based on the edge chosen by the polarity switch (13 pin).

#### Frequency range
- **Frequency range**: 100 Hz to 200 kHz
- **Range switch**: Pin 12: Open or +5 V: 100 Hz to 20 kHz
- **0 V: 1 kHz to 200 kHz**

#### Phase shifter input characteristics
- **Input pin (SHIFTER IN)**: Pin 14
- **Input circuit**: CMOS Schmitt trigger input, pulled up by 50 kΩ resistor
  - +3.5 V to +1.5 V
- **Input voltage**: CMOS (0/5 V) level
- **Single edge (1f) mode**: Raising or falling edge is regarded as a reference
- **Polarity switch input circuit**: CMOS Schmitt trigger input, pulled up at 50 kΩ
- **Polarity switch** (SHIFTER IN POL): Pin 13
  - Open or +5 V: The rising edge regarded as a reference
  - 0 V: The falling edge regarded as a reference
- **Pulse duration**: ≥50 ns
- **Input frequency range**: 100 Hz to 200 kHz
- **Dual edge (2f) mode**: Both rising and falling edge are regarded as a reference
- **Mode setting**: Connected SHIFTER IN (Pin 14) and SHIFTER IN POL (Pin 13)
- **Input frequency waveform**: Duty ratio 50%
- **Input frequency range**: 100 Hz to 100 kHz

#### Voltage control characteristics
- **Control input voltage (Vc IN)**: Pin 1
- **Control method**: Phase shift is specified in the proportion to Vc IN
- **Input resistance**: 100 kΩ ±3% @ DC
- **Control range**: 100° (typ) (−100° to +5 V, +100° to −5 V)
- **Linear control range**: ±90°
- **Voltage control sensitivity**: ±20 V
- **Sensitivity accuracy**: ±1 V

#### Phase shifter output characteristics
- **Output pin**: Pin 18
- **Output circuit**: HCMOS output, 100 Ω series resistor
- **Output voltage**: CMOS (0/5 V) level, load ≥10 kΩ
- **Duty**: 50% ±0.1% (typ) @20 kHz
  - 50% ±0.2% (typ) @200 kHz
- **0/180° switch**: Pin 20
  - Open or +5 V: 0°
  - −180°: 0 V
- **−180° accuracy**: −180° ±0.2% (typ) @20 kHz
  - −180° ±0.2% (typ) @200 kHz

### Phase offset
- **100 Hz to 20 kHz range**: ±0.5 deg. (typ) @ 100 Hz
  - ±0.4 deg. (typ) @ 20 kHz
- **1 kHz to 200 kHz range**: ±0.5 deg. (typ) @ 1 kHz
  - ±3.4 deg. (typ) @ 200 kHz

### Phase offset adjustment
- **Adjustment available by a 20 kΩ external potentiometer (Pin 2)**

### Reference voltage
- **Output**: +5 V (Pin 7, −5 V: Pin 8)
- **Output voltage/accuracy**: ±5 V ±3%
- **Temperature stability**: ±100 ppm/°C (typ)
- **Max. output current**: ±1 mA

### Operating voltage range
- **±15 V: 0–1 V**
- **Quiescent current**: +25 mA (max), +18 mA (typ)
  - −20 mA (max), −12 mA (typ)

### General
- **Specified temperature**: 23°C ±5°C
- **Operating environment**: −20°C to 70°C, 10% RH to 90% RH
- **Storage environment**: −30°C to 80°C, 10% RH to 80% RH
- **Package type**: Type SS20 (20-pin shielded SIP)
- **Dimensions**: 66.7x10.5x19.0 mm (not including protrusions)
- **Weight (NET)**: Approx. 20 g
- **RoHS**: Directive 2011/65/EU

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